

Serial No.: 09/668,407

PATENT APPLICATION  
Docket No.: NC 84,834

## REMARKS

Claims 1-48 are pending in the application. Claims 1-22, 17-27, and 33-43 have been rejected. Claims 12-16, 28-32, and 44-48 have been objected to, but have been held to recite allowable subject matter.

Claims 1, 17, and 33 are amended to recite that the data is or may be transferred between the buffer memory and the packet memory. Support for this amendment is found at page 8, lines 5-6. The amendment clarifies that providing access to the data, as recited in the claims, means that the data is copied from one memory to the other.

## Claim Rejections – 35 U.S.C. § 102

Claims 1-48 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Hochschild et al., US 5,546,391.

Hochschild discloses a packet switch having a central queue for transferring chunks from receivers to transmitters. The central queue has a chunk storage RAM and a continuation chunk pointer RAM to store the links from one chunk to the next in the chunk storage RAM.

Claim 1 is to an apparatus comprising a buffer memory and a packet memory. The buffer memory stores data organized into at least one chunk based on a linked list. The data is associated with a connection identifier corresponding to a channel in a network. The connection identifier identifies a connection in the channel. The data is part of a data stream associated with the connection. The packet memory is coupled to the buffer memory to provide access to the stored data when a transfer condition occurs, such that the data may be transferred between the buffer memory and the packet memory.

In order to make a *prima facie* case of anticipation, the reference must disclose each limitation of the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 2 U.S.P.Q.2d 1051, 1053, 814 F.2d 628, 631 (Fed. Cir. 1987); MPEP 2131. Among other deficiencies, Hochschild does not disclose the limitation in claim 1 that the data may be transferred between the buffer memory and the packet memory. In other words, the same data may stored in both the buffer memory and packet memory in one form or another, or at one time or another. For example, a linked list of chunks may be stored in the buffer memory, and the data in the chunks copied to the packet memory with the chunk headers removed, and vice versa. This data is part of the data stream.

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The Examiner stated that the buffer memory is anticipated by the chunk storage RAM and that the packet memory is anticipated by the continuation chunk pointer RAM. However, only the chunk storage RAM stores data that is part of the data stream, and this data is not transferred to or from the continuation chunk pointer RAM.

Further, Hochschild does not disclose the limitation that the packet memory is of a different type than that of the buffer memory. For example, the buffer memory may be SRAM while the packet memory may be SDRAM. Hochschild does not disclose any such difference. As all the claim limitations of claim 1 are not disclosed in the reference, a *prima facie* case of anticipation has not been made.

Claim 17 is to a method of storing the linked list of chunks in the buffer memory and providing access to the stored data using a packet memory. As above, Hochschild does not disclose that the data is transferred between the buffer memory and the packet memory or that the memories are of different types.

Claim 33 is to a system comprising a channel, a data buffer circuit, an input buffer memory, packet memory, and output buffer memory. The input buffer memory stores the linked list. As above, Hochschild does not disclose that the data may be transferred between the buffer memory and the packet memory or that the memories are of different types.

Claims 2, 8-11, 18, 24-27, 34, and 40-43 depend from and contain all the limitations of claims 1, 17, or 33, and are asserted to distinguish from the reference in the same manner as claims 1, 17, and 33.

#### Claim Rejections – 35 U.S.C. § 103

Claims 3-7, 19-23, and 35-39 have been rejected under 35 U.S.C § 103(a) as being allegedly unpatentable over Hochschild in view of Herring et al. (US 6,542,502).

Claim 3 is to the apparatus of claim one, further comprising a descriptor memory to store descriptor information corresponding to the at least one chunk (claim 2), a controller coupled to the descriptor memory and the buffer memory to control data transfer between the buffer memory and the packet memory using the descriptor information (claim 2), a chunk header to store chunk information associated with the linked list, and a chunk data block to store the data.

Herring discloses a replication method, including chunks having chunk headers.

In order to make a *prima facie* case of obviousness, each claim limitation must be

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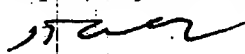
disclosed in the references (MPEP 2143.03). Among other deficiencies, none of the references discloses the limitations in claims 1 (claims 3-7 dependent thereon), 17 (claims 19-23 dependent thereon) and 33 (claims 35-39 dependent thereon) that the data is or may be transferred between the buffer memory and the packet memory and that the packet memory is of a different type than that of the buffer memory. As explained above, these limitations are not disclosed in Hochschild. Neither are the limitations disclosed in Herring. As all the claim limitations of are not disclosed in the references, a *prima facie* case of obviousness has not been made.

Claims 4-7, 20-23, and 36-39 depend from and contain all the limitations of claims 3, 19, or 35, and are asserted to distinguish from the reference in the same manner as claims 3, 19, and 35.

In view of the foregoing, it is submitted that the application is now in condition for allowance.

In the event that a fee is required, please charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please credit Deposit Account No. 50-0281.

Respectfully submitted,



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